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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,930	08/03/2001	Kazuaki Kurooka	401322	8823

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EXAMINER	
BADERMAN, SCOTT T	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,930	KUROOKA ET AL.	
	Examiner	Art Unit	
	Scott T Baderman	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *the communication filed 03 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-10* is/are rejected.

7)☒ Claim(s) *2 and 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 6 and 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 5 is objected to because of the following informalities: In line 3, "said bit width conversion circuit" lacks antecedent basis. It is interpreted as being dependent on claim 4. Appropriate correction is required.

Allowable Subject Matter

3. Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 states, that "if the number of bits of the data on the bus is not larger than a predetermined value, the control circuit stores the data on the bus in only "some" of the trace buffer memories." Being that there are only "two" buffer memories, the above limitation should state only "one" trace buffer memory, as opposed to "some." It is not clear as to what "some" entails. Also, based on the above interpretation, in lines 4-5, "said trace buffer memories" should be "trace buffer memory."

Claim 8 is rejected, as it is dependent on claim 7.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 4-6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (hereinafter "AAPA") in view of Bucher et al. (6,393,587).

As in claims 1 and 6, AAPA discloses a trace circuit built into a debugging circuit that is built into a microcomputer for program debugging, wherein the trace circuit traces data on a bus of the microcomputer according to a bus clock signal and outputting a result to an emulator (Figure 6). AAPA also discloses a trace circuit that comprises a trace buffer memory in which data on the bus of the microcomputer is stored according to the bus clock signal (element 8 of Figure 6), a control circuit storing the data on the bus in the trace buffer memory, cyclically and in a predetermined order, and outputting the data stored in the trace buffer memory, cyclically and in a predetermined order, wherein the storage of data in and output of data from the trace buffer memory is synchronized with the bus clock signal (Figure 6, pp. 1-4), and an output terminal through which the data stored in the trace buffer memory is output to the emulator (Figure 6, pp. 1-4). However, AAPA does not disclose a plural (two) of trace buffer memories. Bucher discloses a protocol analyzer that includes a trace buffer memory, wherein the trace buffer comprises at least two interleaved banks of memory, and wherein the traces are stored in each bank of the trace buffer on alternating clock cycles to enable a sufficient bandwidth between the trace buffer and channel connection to support the high data transfer speeds associated with the fibre channel interface (Abstract, column 4: lines 29-36).

It would have been obvious to a person skilled in the art at the time the invention was made to include a plural (two) of trace buffer memories into the system taught by AAPA above. This would have been obvious because AAPA specifically teaches that due to faster bus clock frequencies in today's microcomputers, the access speed to a trace buffer memory cannot catch up with the speed at which data is transmitted from the control circuit (p. 4). Being that the system taught by Bucher specifically addresses this same issue (column 1: line 48 - column 2:

line 26), and teaches of a trace buffer having two interleaved banks of memory to solve this issue (column 4: lines 29-43), a person skilled in the art would have been led to include two trace buffer memories into the system taught by AAPA to solve the same issue.

As in claims 4 and 9, AAPA discloses that the output control circuit includes a bit width conversion circuit connected between the trace buffer memories and the output terminal, wherein the bit width conversion circuit changes a bit width of the data to be output from the output terminal based on a bit width of the emulator (p. 3).

As in claims 5 and 10, AAPA and Bucher disclose the system above. Further, AAPA discloses an output latch circuit in a number equal to the number of trace buffer memories (i.e., one) and connected between the trace buffer memory and the output control circuit (interpreted as including the bit-width conversion circuit above), wherein the output latch circuit latch outputs of the trace buffer memory (Figure 1, pp. 1-4). Being that the system taught above includes two trace buffer memories, the number of output latch circuits would be two as well.

Conclusion

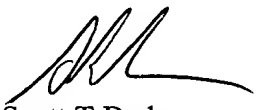
8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Scott T Baderman
Primary Examiner
Art Unit 2113

STB